Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Listing of Claims:

1. (currently amended): A semiconductor chip package, comprising:

a semiconductor chip which includes a through hole extending there through from an active first surface to an inactive second surface;

a first conductive pad which at least partially surrounds the through hole on the active first surface of the semiconductor chip;

a printed circuit board which includes a first surface attached to the inactive second surface of the semiconductor chip, and which further includes a second conductive pad aligned with the through hole of the semiconductor chip; and

a conductive material which fills the through hole and directly contacts the first and second conductive pads.

2. (original): A semiconductor chip package as claimed in claim 1, wherein the conductive material comprises solder.

3. (original): A semiconductor chip package as claimed in claim 2, wherein the solder forms a solder bump over the active first surface of the semiconductor chip.

4. (currently amended): A semiconductor chip package ~~as claimed in claim 1~~, comprising:

a semiconductor chip which includes a through hole extending there through from an active first surface to an inactive second surface;

a first conductive pad which at least partially surrounds the through hole on the active first surface of the semiconductor chip;

a printed circuit board which includes a first surface attached to the inactive second surface of the semiconductor chip, and which further includes a second conductive pad aligned with the through hole of the semiconductor chip; and

a conductive material which fills the through hole and contacts the first and second conductive pads;

wherein the conductive material comprises a metal plug which protrudes into the through hole from the second conductive pad of the printed circuit board, and solder which surrounds the metal plug.

5. (original): A semiconductor chip package as claimed in claim 4, wherein the solder forms a solder bump over the active first surface of the semiconductor chip.

6. (original): A semiconductor chip package as claimed in claim 1, wherein the printed circuit board includes an aperture aligned below the second conductive pad opposite the through hole.

7. (currently amended): A semiconductor chip package as claimed in claim 6 [[4]], further comprising an electrode which is electrically connected to the second conductive pad and which protrudes through the aperture in the printed circuit board.

8. (original): A semiconductor chip package as claimed in claim 7, wherein the electrode is a solder ball.

9. (original): A semiconductor chip package as claimed in claim 1, further comprising an electrode which is electrically connected the second conductive pad and which is attached to a second surface of the printed circuit board opposite the first surface of the printed circuit board.

10. (original): A semiconductor chip package as claimed in claim 9, wherein the electrode is a solder ball.

11. (original): A semiconductor chip package as claimed in claim 1, further comprising an insulating layer located on sidewalls of the through hole of the semiconductor chip.

12. (original): A semiconductor chip package as claimed in claim 1, further comprising an adhesive layer interposed between the inactive second surface of the semiconductor chip and the first surface of the printed circuit board.

13. (original): A semiconductor chip package as claimed in claim 1, further comprising an anisotropic conductive film interposed between the inactive second surface of the semiconductor chip and the first surface of the printed circuit board.

14. (original): A semiconductor chip package as claimed in claim 1, further comprising a protective layer covering the active first surface of the semiconductor chip.

15. (original): A semiconductor multi-package stack, comprising:

a plurality of stacked semiconductor chip packages, each chip package comprising (a) a semiconductor chip which includes a through hole extending there through from an active first surface to an inactive second surface, (b) a first conductive pad which at least partially surrounds the through hole on the active first surface of the semiconductor chip, (c) a printed circuit board which includes a first surface attached to the second surface of the semiconductor chip, and a second conductive pad which is aligned with the through hole of the semiconductor chip, and (d) a conductive material which fills the through hole and contacts the first and second conductive pads.

16. (original): A semiconductor multi-package stack as claimed in claim 15, wherein the semiconductor chip packages are stacked such that the conductive material of a lower chip package contacts the printed circuit board of an adjacent upper chip package.

17. (original): A semiconductor multi-package stack as claimed in claim 16, wherein the conductive material of each semiconductor chip package comprises solder.

18. (original): A semiconductor multi-package stack as claimed in claim 17, wherein the solder forms a solder bump over the active first surface of the semiconductor chip of each semiconductor chip package.

19. (currently amended): A semiconductor multi-package stack ~~as claimed in claim 18~~, comprising a plurality of stacked semiconductor chip packages, each chip package comprising (a) a semiconductor chip which includes a through hole extending there through from an active first surface to an inactive second surface, (b) a first conductive pad which at least partially surrounds the through hole on the active first surface of the semiconductor chip, (c) a printed circuit board which includes a first surface attached to the second surface of the semiconductor chip, and a second conductive pad which is aligned with the through hole of the semiconductor chip, and (d) a conductive material which fills the through hole and contacts the first and second conductive pads;

wherein the semiconductor chip packages are stacked such that the conductive material of a lower chip package contacts the printed circuit board of an adjacent upper chip package, and

wherein the conductive material of each semiconductor chip package comprises a metal plug which protrudes into the through hole from the second

conductive pad of the printed circuit board, and solder which surrounds the metal plug.

20. (original): A semiconductor multi-package stack as claimed in claim 19, wherein the solder forms a solder bump over the active first surface of the semiconductor chip of each semiconductor chip package.

21. (original): A semiconductor multi-package stack as claimed in claim 16, wherein the printed circuit board of each semiconductor chip package includes an aperture aligned below the second conductive pad opposite the through hole, and wherein the conductive material of the lower chip package contacts the second conductive pad of the printed circuit board of the adjacent upper chip package through the aperture of the adjacent upper chip package.

22. (original): A semiconductor multi-package stack as claimed in claim 16, further comprising an electrode which is electrically connected to the second conductive pad a lowermost semiconductor chip package and which protrudes through the aperture in the printed circuit board of the lowermost semiconductor chip package.

23. (original): A semiconductor multi-package stack as claimed in claim 16, wherein the electrode is a solder ball.

24. (original): A semiconductor multi-package stack as claimed in claim 16, further comprising an electrode which is electrically connected the second conductive pad of the lowermost semiconductor chip package of the and which is attached to a second surface of the printed circuit board opposite the first surface of the printed circuit board.

25. (original): A semiconductor multi-package stack as claimed in claim 24, wherein the electrode is a solder ball.

26. (original): A semiconductor chip package as claimed in claim 16, further comprising an insulating layer located on sidewalls of the through hole of the semiconductor chip of each semiconductor chip package.

27. (original): A semiconductor chip package as claimed in claim 16, further comprising an adhesive layer interposed between the inactive second surface of the semiconductor chip and the first surface of the printed circuit board of each semiconductor chip package.

28. (original): A semiconductor chip package as claimed in claim 16, further comprising an anisotropic conductive film interposed between the inactive second surface of the semiconductor chip and the first surface of the printed circuit board of each semiconductor chip package.

29. (original): A semiconductor chip package as claimed in claim 16, further comprising a protective layer covering the active first surface of the semiconductor chip of an uppermost semiconductor chip package.

30. (original): A semiconductor multi-package stack as claimed in claim 15, wherein the semiconductor chip packages are stacked such that the conductive material of an upper chip package contacts the printed circuit board of an adjacent lower chip package.

31. (currently amended): A semiconductor multi-package stack ~~as claimed in claim 30~~, comprising a plurality of stacked semiconductor chip packages, each chip package comprising (a) a semiconductor chip which includes a through hole extending there through from an active first surface to an inactive second surface,

(b) a first conductive pad which at least partially surrounds the through hole on the active first surface of the semiconductor chip, (c) a printed circuit board which includes a first surface attached to the second surface of the semiconductor chip, and a second conductive pad which is aligned with the through hole of the semiconductor chip, and (d) a conductive material which fills the through hole and contacts the first and second conductive pads;

wherein the semiconductor chip packages are stacked such that the conductive material of an upper chip package contacts the printed circuit board of an adjacent lower chip package; and

further comprising an external printed circuit board having a first conductive pad formed on a first surface and a second conductive pad formed on an opposite second surface, and further having an external electrode attached to the second conductive pad, wherein the conductive material of the bottommost semiconductor chip package is attached to the first conductive pad of the external printed circuit board, and wherein the first and second conductive pads of the external printed circuit board are electrically connected.

32. (original): A semiconductor multi-package stack as claimed in claim 31, wherein the external electrode is a solder ball.

33 – 48. (cancelled)

49. (new): A semiconductor chip package, comprising:

a semiconductor chip which includes a through hole extending there through from an active first surface to an inactive second surface;

a first conductive pad which at least partially surrounds the through hole on the active first surface of the semiconductor chip;

a printed circuit board which includes a first surface attached to the inactive second surface of the semiconductor chip, and which further includes a second conductive pad aligned with the through hole of the semiconductor chip; and

a conductive material which fills the through hole and contacts the first and second conductive pads;

wherein the printed circuit board includes an aperture aligned below the second conductive pad opposite the through hole.

50. (new): A semiconductor chip package as claimed in claim 49, further comprising an electrode which is electrically connected to the second conductive pad and which protrudes through the aperture in the printed circuit board.

51. (new): A semiconductor chip package as claimed in claim 50, wherein the electrode is a solder ball.